Modeling of Single Spin Logic Based Hazard Free Network

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Abstract— Modern CMOS based advanced digital circuits suffer unwanted switching transients referred as 'hazard', due to ununilateral propagation delays. The hazard in combinational circuit results from a single variable change when the output should not have been altered or manipulated. The hazardous behavior of the logic circuit often creates a glitch. The glitching effect is negligible in very small circuits but when an extreme sophisticated circuits are made the glitching effect increases manifold. To address such complicated issues a new device principle of operation has come up, namely Single Spin Logic. This particular document shows how a Single Spin Logic based hazard free network is designed with adequate efficiency.

Index Terms— Single Spin Logic, Glitch, Hazard free network, Anti-ferro magnetic, Robustness, Power consumption, Not interconnected

1 INTRODUCTION

PRESENTLY CMOS made VLSI technology is confronted with the Red Brick Wall problem [1], that leads to fatigue the miniaturization process beyond few nanometers. Consequently researchers had to opt for a technological shift. Many new approaches appeared including single electron transistor, hybrid CMOS Single Electron Transistors, Carbon Nano-Tubes, Quantum Electronics etc. But all these are charge coupled devices and all faces power dissipation problem. A new paradigm which is distinctly different from any other charge based devices is the spin logic which involves up-spin and down spin to process 1 bit of information [2], [3], [4], [5].

The Spin logic or more popularly single spin logic [SSL] ushered new hope owing to its inherent properties that is the spin state of the electron remains unaltered in quantum dots compared to any other charge based bulk devices and thus they are quite easier to improvise. This attracted many researchers world-wide and many digital spin based circuit NAND, MUX, XOR, ALU has been reported in reputed scientific journals [6].

On the other hand hazard in many electronic circuits is a natural phenomenon resulting unwanted switching transient and appear at the output of a circuit because of the fact that different paths reflect unidentical propagation delay. This in turn produces spurious spike called glitch. The same is observed both in combinational circuit as well as sequential circuits.The author here are keen to develop SSL made hazard free network.

In order to achieve so the author first realized SSL based hazardous circuits/Gated network and sequently incorporated necessary amenities to resolve the hazardous effect from the same gated network.

2 SSL BASED AOI REALIZATION

In IC designing AOI logic is extremely impetus as it provides unilateral scope to configure complex logic. Following are the AND, OR configuration alongwith XOR in Fig.1, 2 and 3 respectively.

3 PROPOSED MODEL

For easy designing the entire model is subdivided in two categories. First we initialize a hazardous gated network using single spin logic. For simplicity we limited the number of inputs within three. The switching function considered here is F = AC′ + AB′ + BC′. This is achieved in fig.4. The POS form intrinsically reveals the hazard for the above switching function. As this is a compact network it is often referred as cut-set hazard

$$F = (A+B)\,(B+C') \quad \ldots\ldots\ldots\ldots\ldots\ldots (i)$$

Now to make it a hazard free network the equation (i) is realized using SOP form and is expressed as

$$F = AC' + AB' + BC' \quad \ldots\ldots\ldots\ldots\ldots (ii)$$

The same is depicted in Fig. 5. A thorough insight into the spintronic behavior of both the circuits explore the merits of spintronics over conventional CMOS particularly in the field of propagation delay, speed, power consumption and device integrity.

Thus it is revealed that hazard free network is obtained if a function is realized in its original form without restoring it back to its original form of factorizing.

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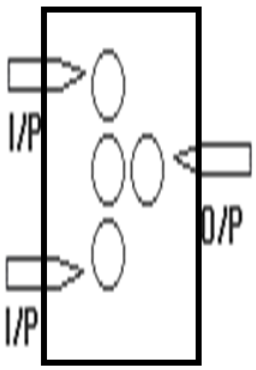

Fig1: SSL based AND gate

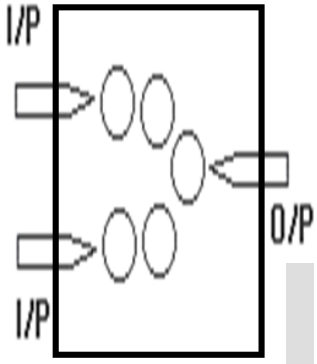

Fig2: SSL based OR gate

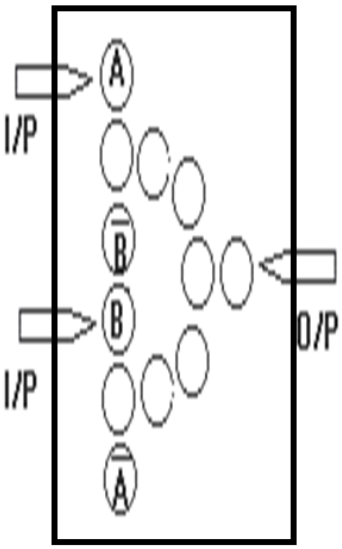

Fig3: SSL based XOR gate

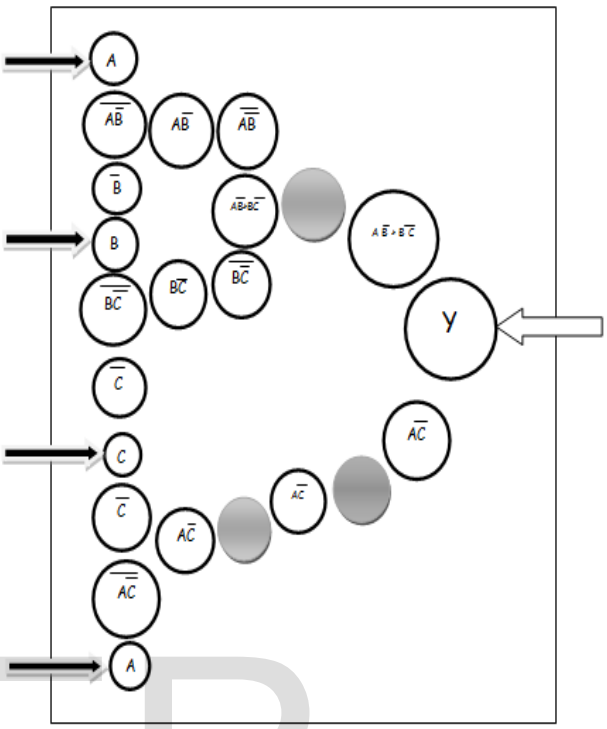

Fig4: SSL based Hazardous gated network

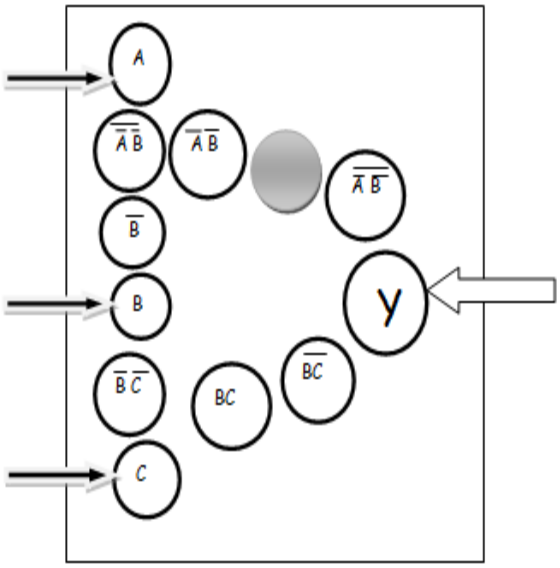

Fig5: SSL based Cut-set hazard gated network

4 CONCLUSION

The authors here adhere to the case study involving hazardous network and hazard free network as well as they wanted to substantiate the merits of SSL over any charged couple devices. Analytical study revealed that SSL logic is a benevolent approach to replace conventional CMOS.

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